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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,220	04/02/2004	Chun-Mai Liu	42236P070C	2432

8791 7590 09/22/2004

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EXAMINER	
LAXTON, GARY L	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/817,220	LIU ET AL.	
	Examiner	Art Unit	
	Gary L. Laxton	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,12-18 and 20-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,12-18 and 20-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Specification

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

3. Claims 1-8, 12-18, 20, 22, 23 and 25 are objected to because of the following informalities:

Claim 1 line 8 recites, "a tap positions" [sic]. Claims 12 and 15 line 6, same problem. Claims 2-8, 13, 14 and 16-18 inherit the same from claims 1, 12 and 15.

Claims 2, 17, 18, 20, 22 and 25 line 3, all reference the phases "coarse adjustment" and "fine adjustment". Coarse and fine are not defined in the claims; therefore, the meets and bounds of those phrases are not identifiable and are not given any patentable weight.

Claim 23 recites "each equal in number an value" [sic].

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 21-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 20 recites the limitation "the two end terminals of a variable impedance network" in line 2. There is insufficient antecedent basis for this limitation in the claim. Furthermore, it is unclear if the applicant is introducing a second variable impedance network or if the applicant is referring to the network referenced in the preamble.

Claim 21 line 2 recites "each connected in series". It is unclear if the applicant means the first and second plurality is connected in series or if each impedance element of each group is connected in series or if all the impedance elements are connected in series. Claims 22-32 inherit the same from claim 21.

Claim 21 recites the limitation "the series connection of the first plurality" and "the series connection of the second plurality" in lines 3 and 4. There is insufficient antecedent basis for these limitations in the claim. Claims 22-32 inherit the same from claim 21.

Claim 21 recites the limitation "the first series connection of the first plurality of impedance elements" in line 5. There is insufficient antecedent basis for this limitation in the claim. Claims 22-32 inherit the same from claim 21.

Claim 21 recites the limitation "the at least one end terminal" in line 2. There is insufficient antecedent basis for this limitation in the claim. Claims 22-32 inherit the same from claim 21.

Claim 24 recites the limitation "the first terminal of the network of claim 23" in line 6 and "the second terminal of the network of claim 23" in line 7. There is insufficient antecedent basis for these limitations in the claim. Furthermore, claim 24 is already dependent on claim 23 as instanced in line 1 of the claim. Still further, this is an improper way of referencing an element in claim 23. It is unclear what the applicant is attempting with the above limitations referencing claim 23.

Claims 26 and 31 recite the limitations "the impedance elements" in line 1 of both claims. There is insufficient antecedent basis for these limitations in the claims. It is unclear which impedance elements are being referenced since several plurality of impedance elements were previously claimed and recited.

Claim 29 recites the limitation "the switching elements" in line 1. There is insufficient antecedent basis for this limitation in the claim. It is unclear which switching elements are being referenced since several plurality of switching elements were previously claimed and recited.

Claim 32 recites the limitation "the resistances at each end" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 32 recites the limitation "the second plurality of resistances" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 32 recites "resistances at each end of the second plurality are reduced". Is this taking place as the circuit operates or is the applicant trying to claim installing smaller resistances on the ends? Is this claim a method of installing smaller resistances on the ends then, or is this an apparatus claim having small resistances on the ends???

Double Patenting

6. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

7. Claims 1, 12 and 15 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-4 of U.S. Patent No. 6,744,244. Although the conflicting claims are not identical, they are not patentably distinct from each other because the instant invention presents broader claims than that of U.S. Patent No. 6,744,244, therefore, U.S. Pat 6,744,244 fully encompasses the instant invention with respect to claims 1, 12 and 15.

8. Claims 2-8, 12-18, 20-23 and 27-32 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-4 of U.S. Patent No. 6,744,244 in view of U.S. Patent No. 6,567,026.

U.S. Pat 6,744,244 discloses an impedance network having an impedance network comprising: a plurality of impedance elements; at least one end terminal; a first plurality of switching elements selectively providing tap positions to the at least one end terminal, selectable at a first specified increment of impedance elements in the plurality of impedance elements; a wiper terminal; and a second plurality of switching elements selectively providing a tap positions to the wiper terminal, selectable at a second specified increment of impedance elements in the plurality of impedance elements.

However, U.S. Pat 6,744,244 does not disclose the following limitations that US Pat 6,567,026 Gorman teaches.

US Pat 6,567,026 Gorman teaches; claim 2, the first specified increment is larger than the second specified increment, to enable the first plurality of switching elements to provide coarse adjustment, and to enable the second plurality of switching elements to provide fine adjustment.

Claim 3; Gorman further discloses wherein the second plurality of switching elements (Sc1-Sc8) is disposed in the middle of the impedance network to allow end-to-end resistance to remain constant.

Claims 4, 27 and 28; US Pat 6,744,244 and US Pat 6,567,026 Gorman discloses the claimed invention except for the first specified increment is four impedance elements. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Gorman to use a first specified increment of four impedance elements, since it has been

held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum value or range involves only routine skill in the art *In re Aller*, 105 USPQ 233; and since discovering an optimum value of a result effective variable involves only routine skill in the art *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980); and further since mere duplication of parts of the essential working pats of a device involves only routine sill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Gorman to use first specified increment of four impedance elements in order to increase the impedance is larger steps without having to use an over sized impedance in place in an attempt to keep the size of the circuit to a minimum.

Claim 5; Gorman further discloses wherein the second specified increment is one.

Claims 6-8; Gorman further discloses wherein the first plurality of switching elements includes a plurality of FET transistors.

Claim 12; Gorman discloses a resistor network (figures 1, 6 and 9) having a plurality of resistors, comprising: at least one end terminal (Vref+, Vref-); a wiper terminal (2); a first plurality of switching elements (Sa1-Sa8 or Sb1-Sb8) selectively providing tap positions to the at least one end terminal, selectable at a first specified increment of resistors in the network; and a second plurality of switching elements (Sc1-Sc8) selectively providing a tap positions to the wiper terminal, selectable at a second specified increment of resistors in the network.

Claims 13 and 14; Gorman further discloses wherein said first set of switching elements includes a plurality of FET transistors.

Claim 15; Gorman discloses a method for configuring an impedance network, comprising: providing a plurality of impedance elements (resistors); providing at least one end terminal (Vref+, Vref-) and a wiper terminal (2); first selectively providing tap positions to the at least one end terminal (Sa1-Sa8 or Sb1-Sb8), selectable at a first specified increment of impedance elements in the network; and second selectively providing a tap positions (Sc1-Sc8) to the wiper terminal (2), selectable at a second specified increment of impedance elements in the network.

Claims 16-18; Gorman further discloses wherein the first and second selectively providing includes selecting the first specified increment to be larger than the second specified increment for course and fine adjustments.

Claim 20; Gorman discloses a method for configuring an impedance network (figure 1, 6, 9), comprising: selectively connecting a first plurality of resistors to two end terminals of a variable impedance network (Vref+, Vref-) for coarse adjustment; selectively connecting a second plurality of resistors (Sc1-Sc8) to the wiper terminal (2) for fine adjustment, and configuring the first and second pluralities of resistors to provide all increments of resistance values.

Claim 21; Gorman discloses an impedance network (figures 1, 6, 9), comprising: first and second pluralities of impedance elements (Sa1-Sa8 connected in series or Sb1-Sb8 connected in series or Sa1-Sa8 connected in series with Sc1-Sc8 or Sb1-Sb8 in series with Sc1-Sc8), one end of the series connection of the first plurality of impedance elements being connected to one end of the series connection of the second plurality of impedance elements (Sa1-Sa8 and Sc1-Sc8 or Sb1-Sb8 and Sc1-Sc8); a first end terminal (Vref+ or Vref-) connected to a second end of the

first series connection of the first plurality of impedance elements; a first plurality of switching elements selectively coupling nodes between impedances in the first plurality of impedance elements to the at least one end terminal (Vref+ or Vref-), selectable at a first specified increment of impedance elements in the first plurality of impedance elements; a wiper terminal (2); and a second plurality of switching elements (Sc1-Sc8) selectively coupling nodes between impedances in the second plurality of impedance elements (Rc1-Rc8) to the wiper terminal (2), selectable at a second specified increment of impedance elements.

Claim 22; Gorman further discloses wherein the first specified increment is larger than the second specified increment, to enable the first plurality of switching elements to provide coarse adjustment, and to enable the second plurality of switching elements to provide fine adjustment.

Claim 23; Gorman further discloses a third plurality of impedance elements (Sb1-Sb8 or Sa1-Sa8), each equal in number and value to the first plurality of impedance elements (Sa1-Sa8 connected in series or Sb1-Sb8 connected in series or Sa1-Sa8 connected in series with Sc1-Sc8 or Sb1-Sb8 in series with Sc1-Sc8), one end of the series connection of the third plurality of impedance elements being connected to a second end of the series connection of the second plurality of impedance elements; a second end terminal connected to a second end of the series connection of the third plurality of impedance elements; and a third plurality of switching elements selectively coupling nodes between impedances in the third plurality of impedance elements to the second end terminal, selectable at a first specified increment of impedance elements in the third plurality of impedance elements; wherein the second plurality of switching

elements is disposed in the middle of the impedance network to allow end-to-end resistance to remain constant.

Claims 29-32; Gorman further discloses wherein said switching elements includes a plurality of FET transistors and the impedance elements are resistances.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify U.S. Pat 6,744,244 with the teachings of US Pat 6,567,026 Gorman; since Gorman essentially disclose the claimed invention.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-3, 5-8, 12-18, 20-23 and 29-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Gorman (US 6,567,026).

Due to the error issues noted above in the claims, as far as the examiner understands the claim language, Gorman is considered to disclose the claimed invention as noted infra.

Claim 1; Gorman discloses an impedance network (figures 1, 6, 9), comprising: a plurality of impedance elements (Resistors); at least one end terminal (Vref+ or Vref-); a first plurality of switching elements (Sa1-Sa8 or Sb1-Sb8) selectively providing tap positions to the at least one end terminal (Vref+ or Vref-), selectable at a first specified increment of impedance elements in the plurality of impedance elements; a wiper terminal (2); and a second plurality of

switching elements (Sc1-Sc8) selectively providing a tap positions to the wiper terminal (2), selectable at a second specified increment of impedance elements in the plurality of impedance elements.

Claim 2; Gorman further discloses wherein the first specified increment is larger than the second specified increment, to enable the first plurality of switching elements to provide coarse adjustment, and to enable the second plurality of switching elements to provide fine adjustment.

Claim 3; Gorman further discloses wherein the second plurality of switching elements (Sc1-Sc8) is disposed in the middle of the impedance network to allow end-to-end resistance to remain constant.

Claim 5; Gorman further discloses wherein the second specified increment is one.

Claims 6-8; Gorman further discloses wherein the first plurality of switching elements includes a plurality of FET transistors.

Claim 12; Gorman discloses a resistor network (figures 1, 6 and 9) having a plurality of resistors, comprising: at least one end terminal (Vref+, Vref-); a wiper terminal (2); a first plurality of switching elements (Sa1-Sa8 or Sb1-Sb8) selectively providing tap positions to the at least one end terminal, selectable at a first specified increment of resistors in the network; and a second plurality of switching elements (Sc1-Sc8) selectively providing a tap positions to the wiper terminal, selectable at a second specified increment of resistors in the network.

Claims 13 and 14; Gorman further discloses wherein said first set of switching elements includes a plurality of FET transistors.

Claim 15; Gorman discloses a method for configuring an impedance network, comprising: providing a plurality of impedance elements (resistors); providing at least one end

terminal (Vref+, Vref-) and a wiper terminal (2); first selectively providing tap positions to the at least one end terminal (Sa1-Sa8 or Sb1-Sb8), selectable at a first specified increment of impedance elements in the network; and second selectively providing a tap positions (Sc1-Sc8) to the wiper terminal (2), selectable at a second specified increment of impedance elements in the network.

Claims 16-18; Gorman further discloses wherein the first and second selectively providing includes selecting the first specified increment to be larger than the second specified increment for course and fine adjustments.

Claim 20; Gorman discloses a method for configuring an impedance network (figure 1, 6, 9), comprising: selectively connecting a first plurality of resistors to two end terminals of a variable impedance network (Vref+, Vref-) for coarse adjustment; selectively connecting a second plurality of resistors (Sc1-Sc8) to the wiper terminal (2) for fine adjustment, and configuring the first and second pluralities of resistors to provide all increments of resistance values.

Claim 21. Gorman discloses an impedance network (figures 1, 6, 9), comprising: first and second pluralities of impedance elements (Sa1-Sa8 connected in series or Sb1-Sb8 connected in series or Sa1-Sa8 connected in series with Sc1-Sc8 or Sb1-Sb8 in series with Sc1-Sc8), one end of the series connection of the first plurality of impedance elements being connected to one end of the series connection of the second plurality of impedance elements (Sa1-Sa8 and Sc1-Sc8 or Sb1-Sb8 and Sc1-Sc8); a first end terminal (Vref+ or Vref-) connected to a second end of the first series connection of the first plurality of impedance elements; a first plurality of switching elements selectively coupling nodes between impedances in the first plurality of impedance

elements to the at least one end terminal (Vref+ or Vref-), selectable at a first specified increment of impedance elements in the first plurality of impedance elements; a wiper terminal (2); and a second plurality of switching elements (Sc1-Sc8) selectively coupling nodes between impedances in the second plurality of impedance elements (Rc1-Rc8) to the wiper terminal (2), selectable at a second specified increment of impedance elements.

Claim 22; Gorman further discloses wherein the first specified increment is larger than the second specified increment, to enable the first plurality of switching elements to provide coarse adjustment, and to enable the second plurality of switching elements to provide fine adjustment.

Claim 23; Gorman further discloses a third plurality of impedance elements (Sb1-Sb8 or Sa1-Sa8), each equal in number and value to the first plurality of impedance elements (Sa1-Sa8 connected in series or Sb1-Sb8 connected in series or Sa1-Sa8 connected in series with Sc1-Sc8 or Sb1-Sb8 in series with Sc1-Sc8), one end of the series connection of the third plurality of impedance elements being connected to a second end of the series connection of the second plurality of impedance elements; a second end terminal connected to a second end of the series connection of the third plurality of impedance elements; and a third plurality of switching elements selectively coupling nodes between impedances in the third plurality of impedance elements to the second end terminal, selectable at a first specified increment of impedance elements in the third plurality of impedance elements; wherein the second plurality of switching elements is disposed in the middle of the impedance network to allow end-to-end resistance to remain constant.

Claims 29-32; Gorman further discloses wherein said switching elements includes a plurality of FET transistors and the impedance elements are resistances.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 4, 27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gorman (US 6,567,026).

Claims 4 and 27; Gorman discloses the claimed invention except for the first specified increment is four impedance elements. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Gorman to use a first specified increment of four impedance elements, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum value or range involves only routine skill in the art *In re Aller*, 105 USPQ 233; and since discovering an optimum value of a result effective variable involves only routine skill in the art *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980); and further since mere duplication of parts of the essential working pats of a device involves only routine sill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Gorman to use first specified increment of four impedance

elements in order to increase the impedance is larger steps without having to use an over sized impedance in place in an attempt to keep the size of the circuit to a minimum.

Claim 28; Gorman discloses the second specified increment is one impedance element.

Allowable Subject Matter

13. Claims 24-26 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter: claim 24 if rewritten in proper form to correct the errors noted above would be considered to contain allowable subject matter stated infra.

Claims 24-26; prior art fails to disclose or suggest, inter alia, an impedance network comprising fourth and fifth pluralities of impedance elements, each being equal in number and impedance to the number and impedance of the impedances in the second plurality of impedance elements; the fourth plurality of impedance elements being coupled in series with one end coupled to a first terminal and a second end coupled to a third terminal; the fifth plurality of impedance elements being coupled in series with one end coupled to a second terminal and a second end coupled to a fourth terminal; a fourth plurality of switching elements selectively coupling nodes between impedances in the fourth plurality of impedance elements to the wiper terminal; and a fifth plurality of switching elements selectively coupling nodes between impedances in the fifth plurality of impedance elements to the wiper terminal.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 6,384,762 Brunolli et al disclose a switched impedance network; US 5,831,566 Ginetti discloses a switched impedance network with 4 strings; US Ikuta et al disclose an impedance network with two series connected impedance elements per leg; US 5,495,245 Ashe discloses an impedance network.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary L. Laxton whose telephone number is (571) 272-2079. The examiner can normally be reached on Monday thru Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2084. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gary L. Laxton
Patent Examiner
Art Unit 2838

9/25/04